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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	**Application No.** 10/535,172	**Applicant(s)** SUBRAMANIAN ET AL.	
	Examiner Scott M. Sciacca	**Art Unit** 2446	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 August 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,11-21 and 24-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,11-21 and 24-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

This office action is responsive to communications filed on August 11, 2008. Claims 11-17 have been amended. Claims 3-10, 22 and 23 have been cancelled. New Claims 25 and 26 have been added. Claims 1, 2, 11-21 and 24-26 are pending in the application.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2, 11-12 and 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schnell (US 5,757,795) in view of Ross (US 5,394,402).

Regarding Claim 1, Schnell teaches a data switch having a plurality of ingress/egress ports (*"The network switch 102 includes two or more input/output (I/O) ports, or "ioports" 104"* – See Col. 5, lines 12-14) and for transmitting data packets including a destination address (*"The network switch 102 operates to receive information from data devices coupled to each of the ioports 104 and to route the information to one or more of the other ioports 104"* – See Col. 5, lines 43-45; *"The data or information is in the form of packets"* – See Col. 5, lines 49-50; *"A packet is a predefined block of bytes, which generally consists of header, data, and trailer"* – See

Col. 5, lines 52-53; *"The header usually includes a source address identifying a data device originating the packet and a destination address identifying the destination data device"* – See Col. 5, lines 54-57), the data switch having address table construction means for generating a table containing associations between ports of the switch and MAC addresses of any devices connected to the switch via those ports (*"The MAC address map 412 is a linked list structure including each MAC address received and the corresponding port number associated with that MAC address"* – See Col. 10, lines 64-66; *"The packet processor 212 receives all packets containing new MAC addresses, and updates the MAC address map 412 and the hash memory 217. A new source MAC address is copied into the MAC address map 412 along with its corresponding port number"* – See Col. 11, lines 21-25).

Schnell does not explicitly teach the address table construction means being operable to construct said table <u>in respect of all but a first one of the ports</u> (emphasis added). However, Ross discloses constructing a table containing associations between ports of the switch and MAC addresses in respect of all but a first port (*"Another function takes the form of means (MAC ADDR) 62 for determining the MAC addresses of each of end stations 20, 22, 24, 26, 28, 30, 32, 34, and 36 (and the MAC addresses of each of internal ports 12, 14, and 16 if such MAC addresses exist) and storing those MAC addresses in memory 42"* – See Col. 5, lines 61-66). Additionally, Ross discloses at Col. 4, lines 63-65 *"FIG. 1 shows a digital data communications network hub 10 in accordance with the invention having three internal ports 12, 14, and 16 and one external port 18."* As Ross shows, the hub has a plurality of ports (internal ports 12, 14

and 16 – See Fig. 1) having several devices (end stations 20, 22, 24, 26, 28, 30, 32, 34, and 36 – See Fig. 1) connected thereto. The MAC addresses of these devices are stored into memory. This is performed for all ports except with respect to a single port (external port 18 – See Fig. 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the switch taught by Schnell to include the functionality of generating a table containing associations between ports of the switch and MAC addresses of any devices connected to the switch in respect of all but a first one of the ports. Ross discloses that internal ports 12, 14 and 16 have end stations directly connected to them (See Col. 5, lines 1-6) and that external port 18 serves the purpose of interconnecting the switch to a backbone network (Col. 6, lines 56-60). One would have been motivated to store associations between ports of a switch and MAC addresses in respect of all but a first one of the ports since the configuration used by Ross provides enhanced security and efficient routing of data across a backbone network to other network segments (See Col. 2, lines 46-52).

Regarding Claim 2, Ross further teaches constructing said table in respect of all of the ports, according to a setting of a control register (*"FIG. 2 is a symbolic block diagram of an illustrative example of FPE 40 in network hub 10"* – See Col. 5, lines 49-50; *"Included within FPE 40 are a number of specific functions which may be either hardware or software implemented"* – See Col. 5, lines 55-57; *"Another function takes the form of means (MAC ADDR) 62 for determining the MAC addresses of each of end*

stations 20, 22, 24, 26, 28, 30, 32, 34, and 36 (and the MAC addresses of each of internal ports 12, 14, and 16 if such MAC addresses exist) and storing those MAC addresses in memory 42" – See Col. 5, lines 61-66; *"FPE 40 preferably takes the form of a software controlled central processing unit"* – See Col. 5, lines 29-31).

Regarding Claim 11, Schnell in view of Ross teaches a device including a data switch according to Claim 1 (See above).

Schnell teaches the plurality of ingress/egress ports comprising a first ingress/egress port (*"FIG. 1 is a simplified network diagram of a network system including a network switch according to the present invention"* – See Col. 4, lines 38-40; IOPORT1 – See Fig. 1) and a plurality of other ingress/egress ports (IOPORT2, … , IOPORTJ – See Fig. 1), and wherein the data switch further comprises:

a table store configured to store a table containing associations between the plurality of other ingress/egress ports and MAC addresses of any devices connected to the switch via the plurality of other ingress/egress ports (*"The MAC address map 412 is a linked list structure including each MAC address received and the corresponding port number associated with that MAC address"* – See Col. 10, lines 64-66);

a switching fabric (*"The network switch further includes switching fabric with a switch controller for controlling transfer of data packets between the network ports and the packet buffers"* – See Col. 3, lines 2-4), and

a control unit operable to control the switching fabric (*"The network switch further includes switching fabric with a switch controller for controlling transfer of data packets between the network ports and the packet buffers"* – See Col. 3, lines 2-4).

Schnell does not explicitly teach the control unit being arranged, upon receiving a data packet from any of the other ingress/egress ports having a destination address which is not stored in the table, to control the switching fabric to transmit the data packet to the first ingress/egress port. However, Ross teaches a network switch having a first ingress/egress port (external port 18 – See Fig. 1) and a plurality of other ingress/egress ports (internal ports 12, 14 and 16 – See Fig. 1) and storing MAC address associations in a table (*"Another function takes the form of means (MAC ADDR) 62 for determining the MAC addresses of each of end stations 20, 22, 24, 26, 28, 30, 32, 34, and 36 (and the MAC addresses of each of internal ports 12, 14, and 16 if such MAC addresses exist) and storing those MAC addresses in memory 42"* – See Col. 5, lines 61-66). Ross also discloses receiving a data packet from any of the other ingress/egress ports having a destination address which is not stored in the table and transmitting the data packet to the first ingress/egress port (*"In operation, when a message is received from an internal port, the FPE 40 accesses the MEM 42 in order to associate a VLAN designation with the message based on the internal port from whence it came, and in addition, by using the unique MAC address in the DA field 82 of the message, learns if the end station with the unique address matching that DA is located on one of the internal ports of the hub"* – See Col. 9, lines 44-51; *"The end station with that DA is not located on one of the other internal ports on the same hub. In*

this instance, the message with the VLAN designation appended is encapsulated in the appropriate format by the FPE 40 and forwarded to the external port for transmission on the backbone network" – See Col. 10, lines 3-8). Ross constructs a table that stores MAC addresses associated with all devices connected to internal ports 12, 14 and 16 (other ingress/egress ports). When a packet is received which has a destination address not listed in the table, the packet is forwarded to the external port 18 (first ingress/egress port) for transmission over a backbone network.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the control of the switching fabric taught by Schnell to include controlling the switching fabric to transmit the data packet to the first ingress/egress port when a data packet having a destination address which is not stored in the table is received. One would have been motivated to do so since Ross discloses that it is an efficient way of transmitting data across a backbone network to other network segments (See Col. 2, lines 46-52).

Regarding Claim 12, Ross further teaches the first ingress/egress port (external port 18 – See Fig. 1) being adapted to be connected to a communication network (*"The important point is that at least selected portions of backbone network 76 are shared by all messages transmitted contemporaneously from any of external ports 18, 118, and 218"* – See Col. 6, lines 56-60).

Regarding Claim 24, Schnell teaches a method of operating a data switch for switching data packets including a destination address, the data switch comprising a plurality of ingress/egress ports (IOPORT1, IOPORT2, ... , IOPORTJ – See Fig. 1), the method comprising:

generating a table containing associations between ports of the switch and MAC addresses of any devices connected to the switch via those ports (*"The packet processor 212 initializes the MAC address map 412 and the hash memory 217 upon power up"* – See Col. 11, lines 9-10; *"The MAC address map 412 is a linked list structure including each MAC address received and the corresponding port number associated with that MAC address"* – See Col. 10, lines 64-66; *"The packet processor 212 receives all packets containing new MAC addresses, and updates the MAC address map 412 and the hash memory 217. A new source MAC address is copied into the MAC address map 412 along with its corresponding port number"* – See Col. 11, lines 21-25).

Schnell does not explicitly teach the generation of the table including constructing said table in respect of all but a first one of the ports. However, Ross discloses a first port (external port 18 – See Fig. 1) and a plurality of other ports (internal ports 12, 14 and 16 – See Fig. 1). Additionally, Ross teaches generation of a MAC address table including constructing said table in respect of all but a first one of the ports (*"Another function takes the form of means (MAC ADDR) 62 for determining the MAC addresses of each of end stations 20, 22, 24, 26, 28, 30, 32, 34, and 36 (and the MAC addresses of each of internal ports 12, 14, and 16 if such MAC addresses exist) and storing those*

MAC addresses in memory 42" – See Col. 5, lines 61-66). As Ross shows, the hub has a plurality of ports (internal ports 12, 14 and 16 – See Fig. 1) having several devices (end stations 20, 22, 24, 26, 28, 30, 32, 34, and 36 – See Fig. 1) connected thereto. The MAC addresses of these devices are stored into memory. This is performed for all ports except with respect to a single port (external port 18 – See Fig. 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the switch taught by Schnell to include the functionality of generating a table containing associations between ports of the switch and MAC addresses of any devices connected to the switch in respect of all but a first one of the ports for the same reasons as those given with respect to Claim 1.

Regarding Claim 25, Ross teaches the plurality of ingress/egress ports including a plurality of other ingress/egress ports (internal ports 12, 14 and 16 – See Fig. 1), and wherein the data switch further comprises a memory storing a table containing associations between the other ingress/egress ports and MAC addresses of any devices connected to the switch via the other ingress/egress ports (*"Network hub 10 further includes a flow processing element (FPE) 40 and a local memory 42 for storing VLAN designations for internal ports 12, 14, and 16, media access control (MAC) addresses for end stations 20, 22, 24, 26, 28, 30, 32, 34, and 36"* – See Col. 5, lines 14-18), the method further comprising:

receiving a data packet from any of the other ingress output ports (*"a message is received from an internal port"* – See Col. 9, lines 44-45), and

transmitting the data packet to the first ingress/egress port if the data packet contains a destination address that is absent from the table (*"by using the unique MAC address in the DA field 82 of the message"* – See Col. 9, lines 48-49; *"The end station with that DA is not located on one of the other internal ports on the same hub. In this instance, the message with the VLAN designation appended is encapsulated in the appropriate format by the FPE 40 and forwarded to the external port for transmission on the backbone network"* – See Col. 10, lines 3-8; The MAC address in the DA field of a message is examined. If the MAC address is not one of the addresses of one of the devices located on one of the internal ports, the message is forwarded to the external port).

Regarding Claim 26, Ross teaches transmitting the data packet to a corresponding ingress/output port if the data packet contains a destination address that is present on the table (*"a message is received from an internal port"* – See Col. 9, lines 44-45; *"by using the unique MAC address in the DA field 82 of the message"* – See Col. 9, lines 48-49; *"The end station with that DA is located on one of the other internal ports on the same hub"* – See Col. 9, lines 59-60; *"In this instance, the FPE forwards the message to the appropriate internal port"* – See Col. 9, lines 63-64).

3. Claims 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schnell (US 5,757,795) in view of Ross (US 5,394,402) and further in view of Kramer et al. (US 6,658,027).

Regarding Claim 13, Schnell and Ross do not explicitly teach at least one of the other ingress/egress ports being arranged to receive and transmit voice signals. Schnell discloses the switch being operable to receive and transmit Ethernet data (*"the Ethernet protocol includes a variety of data rates and speeds. Any particular data rate may be used at any particular ioport 104"* – See Col. 17, lines 40-44). Kramer teaches modulating voice signals into Ethernet data (Fig. 3 shows a VoIP apparatus which converts a voice signal via CODEC 160 to Ethernet data via Ethernet interface 310). It would have been obvious to one of ordinary skill in the art at the time the invention was made to convert voice signals to Ethernet data for use with the network switch disclosed by Schnell. Motivation for doing so would be to carry voice signals and other data over the same network infrastructure.

Regarding Claim 14, Kramer further teaches the device comprising a microphone, a speaker, circuitry configured to transform sound signals received from the microphone into data packets and to transform data packets into control signals for the speaker (Fig. 3 shows a microphone, speaker, CODEC 160 and various other circuitry used to convert analog voice signals to digital packet data as well as convert digital packet data to audio signals for playback through a speaker), and wherein the circuitry is coupled to the at least one of the other ingress/egress ports arranged to receive and transmit voice signals (Fig. 3 shows Ethernet interface 310 which may be coupled one of the ingress/egress ports of the Ethernet switch disclosed by Schnell).

Regarding Claim 15, Schnell further teaches sockets adapted to connect one or more of the other ingress/egress ports to devices which each have a MAC address (*"A network switch for transferring data packets according to the present invention includes a plurality of network ports, a plurality of packet buffers, and a switch matrix coupled to each of the network ports"* – See Col. 2, lines 63-66; *"In the specific embodiment described herein, the binary address values are media access control (MAC) addresses used for uniquely identifying network devices"* – See Col. 3, lines 29-31).

Regarding Claim 16, Ross teaches the first ingress/egress port (external port 18 – See Fig. 1) being adapted to be connected to a communications network (*"The important point is that at least selected portions of backbone network 76 are shared by all messages transmitted contemporaneously from any of external ports 18, 118, and 218"* – See Col. 6, lines 56-60).

4. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schnell (US 5,757,795) in view of Khill (US 7,154,899).

Regarding Claim 17, Schnell teaches a method of operating a data switch comprising a first ingress/egress port (*"FIG. 1 is a simplified network diagram of a network system including a network switch according to the present invention"* – See

Col. 4, lines 38-40; IOPORT1 – See Fig. 1) and a plurality of other ingress/egress ports (IOPORT2, ... , IOPORTJ – See Fig. 1), the method including:

generating a table containing associations between at least the plurality of other ingress/egress ports of the switch and MAC addresses of any devices connected to the switch thereby (*"The packet processor 212 initializes the MAC address map 412 and the hash memory 217 upon power up"* – See Col. 11, lines 9-10; *"The MAC address map 412 is a linked list structure including each MAC address received and the corresponding port number associated with that MAC address"* – See Col. 10, lines 64-66; *"The packet processor 212 receives all packets containing new MAC addresses, and updates the MAC address map 412 and the hash memory 217. A new source MAC address is copied into the MAC address map 412 along with its corresponding port number"* – See Col. 11, lines 21-25).

Schnell does not explicitly teach stopping generation of the table before MAC addresses of at least some devices operably coupled through the first ingress/egress port are associated with the first ingress/egress port in the table. However, Khill discloses stopping generation of a MAC address table before MAC addresses of at least some devices operably coupled through a first ingress/egress port are associated with the first ingress/egress port in the table (*"The learning process observes the source addresses of frames received on each port, and dynamically updates the filtering database (conditionally on the state of the receiving port). It either creates or updates an entry in the filtering database, associating the port on which the frame was received with the frame's source MAC address"* – See Col. 1, lines 59-65; *"In preferred embodiments*

of the present invention, the learning process carried out by a virtual bridge is limited to modifying only a portion of the shared filtering database in a period of time, referred to as the learning period" – See Col. 4, lines 14-17; *"Bridge 10 complies with the above-mentioned IEEE standards 802.1D and 802.1Q, but uses a budgeted learning process 12"* – See Col. 5, lines 42-44; *"The method of FIG. 2 is initiated when bridge 10 receives a packet with an unknown source address, at a packet reception step 26. The source address is unknown in the sense that there is no entry in filtering database 14 corresponding to that address"* – See Col. 6, lines 26-30; *"If the budget of entries is exhausted at budget exhaustion test step 32, the learning process terminates for this domain until the current learning period is over, without adding the entry to the filtering database"* – See Col. 6, lines 44-47).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to stop generation of a table before MAC addresses of at least some devices operably coupled through a port are associated with the port in the table. Motivation for doing so would be to prevent certain malicious attacks on a network, such as a denial of service (DOS) attack (See Col. 4, lines 26-29 in Khill).

Regarding Claim 18, Khill teaches stopping generation of the table occurring after at least one MAC address of at least one device operably coupled through a first ingress/egress port is associated with the first ingress/egress port in the table (*"If the budget is not exhausted, learning process 12 adds a new entry into database 14, at an add entry step 34"* – See Col. 6, lines 39-40).

5. Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schnell (US 5,757,795) in view of Khill (US 7,154,899) and further in view of Ross (US 5,394,402).

Regarding Claim 19, Schnell and Khill do not explicitly teach forwarding the data packet to the first ingress/egress port when a data packet having a destination port MAC address absent from the generated table is received. However, Ross teaches a network switch having a first ingress/egress port (external port 18 – See Fig. 1) as claimed in Claim 17 and a plurality of other ingress/egress ports (internal ports 12, 14 and 16 – See Fig. 1) as claimed in Claim 17 and storing MAC address associations in a table (*"Another function takes the form of means (MAC ADDR) 62 for determining the MAC addresses of each of end stations 20, 22, 24, 26, 28, 30, 32, 34, and 36 (and the MAC addresses of each of internal ports 12, 14, and 16 if such MAC addresses exist) and storing those MAC addresses in memory 42"* – See Col. 5, lines 61-66). Ross also discloses receiving a data packet having a destination address which is not stored in the table and transmitting the data packet to the first ingress/egress port (*"In operation, when a message is received from an internal port, the FPE 40 accesses the MEM 42 in order to associate a VLAN designation with the message based on the internal port from whence it came, and in addition, by using the unique MAC address in the DA field 82 of the message, learns if the end station with the unique address matching that DA is located on one of the internal ports of the hub"* – See Col. 9, lines 44-51; *"The end*

station with that DA is not located on one of the other internal ports on the same hub. In this instance, the message with the VLAN designation appended is encapsulated in the appropriate format by the FPE 40 and forwarded to the external port for transmission on the backbone network" – See Col. 10, lines 3-8).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to transmit a data packet to a first ingress/egress port when a data packet having a destination address which is not stored in the table is received for the same reasons as those given with respect to Claim 11.

Regarding Claim 20, Ross further teaches forwarding the data packet further comprising forwarding the data packet only if the data packet was received from one of the plurality of other ingress/egress ports (*"a digital data communications network hub for use in a shared transmission media access LAN includes at least one internal port for receiving and transmitting messages within the hub"* – See Col. 3, lines 8-12).

6. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schnell (US 5,757,795) in view of Khill (US 7,154,899) and further in view of Ross (US 5,394,402) and still further in view of Kramer et al. (US 6,658,027).

Regarding Claim 21, Schnell, Khill and Ross do not explicitly teach converting analog audio signals to data packets and providing the data packets to one of the other ingress/egress ports. However, Kramer teaches converting analog audio signals to

data packets (*"For VoIP networks, audio signals are digitized into frames and transmitted as packets over an IP network"* – See Col. 1, lines 12-13 Fig. 3 shows a CODEC 160 for receiving analog audio data from a microphone and encoding the data into digital packet data) and providing the data packets to one of the other ingress/egress ports (Fig. 3 Shows an Ethernet interface 310 for providing the packet data to a network). It would have been obvious to one of ordinary skill in the art at the time the invention was made to convert voice signals to Ethernet data for use with the network switch disclosed by Schnell for the same reasons as those given with regard to Claim 13.

Response to Arguments

7. Applicant's arguments filed on August 11, 2008 have been fully considered but they are not persuasive.

On page 9 of the remarks, Applicant argues "One example of a limitation of claim 1 that is not taught or suggested by the cited references is that of 'address table construction means for generating a table containing associations between [i] ports of the switch and [ii] MAC addresses of any devices connected to the switch via those ports'. Another example of a limitation that is not taught or suggested by the cited references is that of 'the address table construction

means being operable to construct said table in respect of all but a first one of the ports'."

The feature of an "address table construction means for generating a table containing associations between ports of the switch and MAC addresses of any devices connected to the switch via those ports" is clearly taught by Schnell, as shown above with respect to Claim 1. At Col. 10, lines 64-66, Schnell states *"The MAC address map 412 is a linked list structure including each MAC address received and the corresponding port number associated with that MAC address".* At Col. 11, Schnell states *"The packet processor 212 receives all packets containing new MAC addresses, and updates the MAC address map 412 and the hash memory 217. A new source MAC address is copied into the MAC address map 412 along with its corresponding port number".* The packet processor 212 (address table construction means) generates a table containing associations between a MAC address and a corresponding port number by adding associations to the table each time a packet is received having a previously unseen MAC address.

With respect to the feature of "the address table construction means being operable to construct said table in respect of all but a first one of the ports", Examiner stated above with respect to Claim 1 that Schnell did not explicitly teach this feature. However, Ross describes a switch (hub 10 – See Fig. 3) having a first port (external port 18 – See Fig. 3) and a plurality of other ports (internal ports 12, 14 and 16 – See Fig. 3). At Col. 5, lines 61-66, Ross shows how only MAC addresses associated with

each of the internal ports are stored in memory. At Col. 9, lines 28-35, Ross states *"Also stored in MEM 42, and associated with each of the internal ports may be the unique MAC addresses of all of the end stations that are attached to each particular internal port. These are stored so that when the FPE 40 accesses MEM 42 using the unique MAC address, MEM 42 returns the number of the internal port and the VLAN designation associated with it."* Thus, Ross provides for a MAC address table that stores the actual associations between MAC addresses and the internal port ("other port") associated with them. Ross does this by accessing MEM 42 using a specified MAC address. MEM 42 then returns the internal port number associated with the specified address. Applying this concept to the MAC address map 412 taught by Schnell yields a table that only stores associations between a plurality of "other ports" and the MAC addresses of the devices connected to those ports.

The same reasoning applies to the arguments given with respect to Claim 24.

On page 12 of the remarks, Applicant argues "One example of a limitation of claim 17 that is not disclosed in Schnell or Khill is that of 'stopping generation of the table before MAC addresses of at least some devices operably coupled through the first ingress/egress port are associated with the first ingress/egress port in the table'."

The language of the claim mentions actions performed with respect to a "first ingress/egress port". Due to the absence of any language in the claim that suggests

that the step in question is exclusively performed only with respect to a "first ingress/egress port", Examiner has given the claim the interpretation that the step of "stopping generation of the table" may be performed with respect to any or all ports on a switch. Khill teaches stopping generation of a MAC address table before MAC addresses of at least some devices operably coupled through a port are associated with the port in the table (*"The learning process observes the source addresses of frames received on each port, and dynamically updates the filtering database (conditionally on the state of the receiving port). It either creates or updates an entry in the filtering database, associating the port on which the frame was received with the frame's source MAC address"* – See Col. 1, lines 59-65; *"In preferred embodiments of the present invention, the learning process carried out by a virtual bridge is limited to modifying only a portion of the shared filtering database in a period of time, referred to as the learning period"* – See Col. 4, lines 14-17; *"If the budget of entries is exhausted at budget exhaustion test step 32, the learning process terminates for this domain until the current learning period is over, without adding the entry to the filtering database"* – See Col. 6, lines 44-47).

According to Khill, when a packet is received which has a source MAC address not yet stored in the database (table), the address may only be entered into the database during a learning period. If the learning period has already expired when a packet having a new source MAC address is received, the address will not be entered into the database. Thus generation of the table is stopped before a MAC address of at least one device coupled through a port is associated with the port.

Furthermore, the fact that applicant has recognized another advantage which would flow naturally from following the suggestion of Khill cannot be the basis for patentability when the differences would otherwise be obvious. See Ex parte Obiaya, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985).

Conclusion

1. Applicant's amendment necessitated the new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott M. Sciacca whose telephone number is (571) 270-

1919. The examiner can normally be reached on Monday thru Friday, 7:30 A.M. - 5:00 P.M. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeff Pwu can be reached on (571) 272-6798. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Scott M. Sciacca/
Examiner, Art Unit 2446

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Supervisory Patent Examiner, Art Unit 2446